IN THE CLAIMS

Cancel the present claims 1-4 without prejudice.

Please amend the claims as follows:

1-4. (canceled)

5. (currently amended) An apparatus, comprising:

a ~~networking system~~ network node that executes a series of scheduling cycles in order to allocate switching or routing bandwidth within ~~said~~ a networking system, wherein a highest speed grade is identified for a highest amount of allocated bandwidth, and wherein ~~a unique~~ lower speed grades ~~is~~ are identified for ~~each unique~~ speeds that ~~is~~ are less than ~~said~~ the highest amount of allocated bandwidth, wherein each of ~~said~~ the scheduling cycles is divided ~~partitioned~~ into equal amounts of data, wherein each of the speed grades has a respective bandwidth allocation associated with a respective length of time, ~~bandwidth allotment is provided one of said amounts of data per unit of time,~~ wherein ~~said unit~~ the length of time is one of ~~said~~ the scheduling cycles for ~~said highest amount of allocated bandwidth, and~~ the bandwidth allocation for the highest speed grade, wherein ~~said unit~~ the length of time is more than one of ~~said~~ the scheduling cycles for each bandwidth allocation ~~having a~~ for the lower speed grades, ~~such that~~ wherein ~~its~~ the lower speed ~~is realized~~ grades and the highest speed grade are serviced by the node.

6. (currently amended) The apparatus of claim 5, wherein ~~said unit~~ the length of time for the bandwidth allocation for the highest speed grade is determined with a counting modulo~~, said counting modulo being:~~ comprising the minimum integer derived from

~~$x_1$ = min integer~~[B[[/]] divided by X]~~,~~ ~~for a said highest speed grade bandwidth allotment, where~~ wherein B is ~~said~~ switching or routing capacity of ~~said networking system~~ the networking node and X is ~~said~~ the highest amount of allocated bandwidth.

3 1 ~~7~~. (currently amended) The apparatus of claim ~~5~~ 1 wherein ~~said unit~~ the length of time for each respective bandwidth allocation for the lower speed grades is determined with a counting modulo~~, said counting modulo being~~ comprising

~~$x_n$=k~~ times $x_{n-1}$~~, for a lower speed grade bandwidth allotment, where~~ wherein k is ~~the number of said~~ how many lower speed grade bandwidth ~~allotments that~~ allocations can be provided by a next highest speed grade, and ~~where~~ wherein $x_{n-1}$ is ~~the count~~ a counting modulo for ~~said~~ a next highest speed grade.

4 1 ~~8~~. (currently amended) The apparatus of claim ~~5~~ 1 wherein ~~said networking system said~~ the network node allocates ~~said~~ bandwidth to one or more ports on a port-by-port basis, each of ~~said~~ the ports having one or more queues for queueing packet identifiers that point to where a corresponding packet is found within a memory.

5 4 ~~9~~. (currently amended) The apparatus of claim ~~8~~ 4 wherein ~~said networking system~~ the network node can be configured such that one port exists for each user being serviced by ~~said networking system~~ the network node.

6 4 ~~10~~. (currently amended) The apparatus of claim ~~8~~ 4 wherein ~~said networking system~~ the network node further comprises a scheduler that provides ~~a~~ release signals to ~~each of said~~ the one or more ports at rates in accordance with the respective lengths

of time for the respective bandwidth allocations for the highest speed grade and the lower speed grades, ~~per said unit of time,~~ in order to trigger ~~a~~ releases of ~~said one of said amounts of~~ data from ~~said~~ the memory, ~~said~~ the releases from ~~said~~ the memory in the form of packets pointed to by those of ~~said~~ the packet identifiers stored within ~~said~~ the one or more ports that receives ~~said~~ the release signals.

~~11~~ 7. (currently amended) The apparatus of claim ~~10~~ 6, wherein ~~said networking system~~ the network node further comprises a second memory that can be configured to maintain a separate data entry for each of ~~said~~ the one or more ports, each of ~~said~~ the data entries identifying its corresponding port so that a ~~said~~ release signal to be received by ~~said~~ the corresponding port can be generated by reading its data entry from ~~said~~ the second memory.

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~~12~~ 8. (currently amended) The apparatus of claim ~~11~~ 7, wherein those data entries for each of ~~said~~ the one or more ports having the same data rate are circularly link listed so that release signals to ports having ~~the~~ a same associated speed grade are generated in a circular fashion.

~~13~~ 9. (currently amended) The apparatus of claim ~~12~~ 8, wherein each of ~~said~~ the data entries further comprises space reserved for at least a bit of information that marks whether or not ~~it~~ the data entry is to be recognized as an end of the circular link list to which it belongs.

10 6
14. (currently amended) The apparatus of claim 10, wherein ~~said~~ the scheduler is implemented with application specific logic.

11 6
15. (currently amended) The apparatus of claim 10, wherein ~~said~~ the scheduler is implemented with a processor that executes a software program.

12
16. (currently amended) A method for allocating bandwidth, comprising:

~~executing a series of scheduling cycles in order to allocate switching or routing bandwidth within a networking system, wherein~~

identifying a highest speed grade ~~is identified~~ for a highest amount of allocated bandwidth; ~~and wherein~~

identifying ~~a unique~~ lower speed grades ~~grade is identified~~ for ~~each unique speed~~ speeds that ~~is~~ are less than ~~said~~ the highest amount of allocated bandwidth; ~~each of said~~ dividing each of the scheduling cycles ~~partitioned~~ into equal amounts of data;

providing each of the speed grades with a respective bandwidth allocation associated with a respective length of time,

wherein each bandwidth allotment is provided one of the amounts of data per unit of time, wherein ~~said unit~~ the length of time is one of ~~said~~ the scheduling cycles for ~~said highest amount~~ the bandwidth allocation for the highest speed grade, ~~of allocated bandwidth, and~~ wherein ~~said unit~~ the length of time is more than one of ~~said~~ the scheduling cycles for each bandwidth allocation ~~having a~~ for the lower speed ~~grade~~ grades;wherein ~~such that its~~ the lower speed grades ~~is realized.~~ and the highest speed grade are serviced.

13 12
~~17~~. (currently amended) The method of claim ~~16~~, wherein ~~said unit~~ the length of time for the bandwidth allocation for the highest speed grade is determined with a counting modulo comprising the minimum integer from~~, said counting modulo being:~~

~~$x_1$ = min integer~~[B[[/]] divided by X~~] for a said highest speed grade bandwidth allotment,~~ whereinwhere B is ~~said~~ switching or routing capacity of a network node ~~said networking system~~ and X is ~~said~~ the highest amount of allocated bandwidth.

14 12
~~18~~. (currently amended) The method of claim ~~16~~, wherein ~~said unit~~ the length of time for each respective bandwidth allocation for the lower speed grades is determined with a counting modulo~~, said counting modulo being:~~ comprising

[[$x_n$=]]K times $X_{n-1}$~~, for a lower speed grade bandwidth allotment, where~~ wherein k is ~~the number of said~~ how many lower speed grade bandwidth ~~allotments that~~ allocations can be provided by a next highest speed grade, and ~~where~~ wherein $x_{n-1}$ is ~~the count~~ a counting modulo for ~~said~~ a next highest speed grade.

15 12
~~19~~. (currently amended) The method of claim ~~16~~, further comprising allocating ~~said~~ bandwidth to one or more ports on a port-by-port basis by providing ~~a~~ release ~~signal, per said unit of time,~~ signals to ~~each of said~~ the one or more ports at rates in accordance with the respective lengths of time for the respective bandwidth allocations for the highest speed grades and the lower speed grades, each of ~~said~~ the ports having one or more queues for queueing packet identifiers that point to where a corresponding packet is found within a memory~~, each said release signal provided per said unit of time~~.

16 15
20. (currently amended) The method of claim 19, further comprising triggering a release of ~~said one of said amounts of~~ data from ~~said~~ the memory, ~~said~~ the release from ~~said~~ the memory in the form of packets pointed to by those of ~~said~~ the packet identifiers stored within ~~said~~ a port that receives ~~said~~ a release signal.

17 15
21. (currently amended) The method of claim 19, further comprising configuring ~~said~~ a networking system such that one port exists for each user being serviced by ~~said~~ the networking system.

18 15
22. (currently amended) The method of claim 19, further comprising reading a data entry from a second memory, ~~said~~ the second memory configured to maintain a separate data entry for each of ~~said~~ the one or more ports, each of ~~said~~ the data entries identifying its corresponding port so that a ~~said~~ release signal to be received by ~~said~~ the corresponding port can be generated by ~~said~~ the reading.

19 18
23. (currently amended) The method of claim 22, further comprising generating release signals to ports having ~~the~~ a same associated speed grade in a circular fashion, wherein data entries for each of ~~said~~ the one or more ports having ~~the~~ a same data rate are circularly link listed so that ~~said~~ the circular generation of release signals results.

20
24. (currently amended) ~~An apparatus~~ A network node, comprising:

~~a networking system having~~ one or more ports that each comprise one or more queues for queueing packet identifiers, each of said packet identifiers indicating where

a packet can be found in a buffer memory, each of ~~said~~ the one or more ports having its own data rate so that a plurality of data rates can exist, ~~said networking system capable of calculating a series of scheduling cycles~~, wherein each of ~~said~~ a series of scheduling cycles is partitioned into equal amounts of data, wherein one of ~~said~~ the amounts of data per ~~said~~ scheduling cycle corresponds to a highest data rate of ~~said~~ the plurality of data rates, ~~and~~ wherein, each of ~~said~~ the one or more ports triggers a release from ~~said~~ the buffer memory of one of ~~said~~ the amounts of data worth of its identified packets in response to reception of a release signal derived from ~~said~~ the series of scheduling cycles, and wherein releases from a same port are separated in time so that ~~said same port's~~ a data rate of that same port is realized.

21 20
~~25~~. (currently amended) The ~~apparatus~~ network node of claim ~~24~~, ~~wherein said networking system~~ further ~~comprises~~ comprising a second memory that can be configured to maintain a separate data entry for each of ~~said~~ the one or more ports, each of ~~said~~ the data entries identifying its corresponding port so that a ~~said~~ release signal to be received by ~~said~~ the corresponding port can be generated by reading its data entry from ~~said~~ the second memory.

22 21
~~26~~. (currently amended) The ~~apparatus~~ network node of claim ~~25~~, wherein those data entries for each of ~~said~~ the one or more ports having the same data rate are circularly link listed so that release signals for a particular speed grade are generated in a circular fashion.

23 27. (currently amended) The ~~apparatus~~ network node of claim 22 26, wherein each of ~~said~~ the separate data entries further comprises ~~space reserved for~~ at least a bit of information that marks whether or not ~~it~~ the data entry is to be recognized as an end of the circular link list to which ~~it~~ the data entry belongs.

24 21 28. (currently amended) The ~~apparatus~~ network node of claim 26, further comprising a scheduler that generates ~~said~~ release signals by ~~said~~ reading of ~~said~~ data entries from ~~said~~ the second memory, ~~said~~ the scheduler coupled to each of ~~said~~ the one or more ports so that ~~said~~ the release signals can be issued to ~~said~~ the one or more ports.

25 24 29. (currently amended) The ~~apparatus~~ network node of claim 28, wherein ~~said~~ the scheduler is implemented with application specific logic.

26 24 30. (currently amended) The ~~apparatus~~ network node of claim 28, wherein ~~said~~ the scheduler ~~is implemented with~~ comprises a processor that executes a software program.

27 20 31. (currently amended) The ~~apparatus~~ network node of claim 24, wherein ~~said networking system can be configured to allocate~~ the one ~~of said~~ or more ports ~~to each user~~ are allocated to respective users that ~~is~~ are serviced by ~~said~~ a networking system.

28 27
32. (currently amended) The ~~apparatus~~ network node of claim 31, wherein ~~said~~ the one or more ports and ~~said~~ the buffer memory are part of a networking/transport layer within ~~said~~ the networking system that can[[:]]

1) identify which user an incoming packet is to be sent to; and

2) ~~enters~~ enter a packet identifier into a port that has been allocated to ~~said~~ the user ~~said~~ the incoming packet is to be sent to, ~~said~~ the packet identifier identifying where in ~~said~~ the buffer memory ~~said~~ the incoming packet can be found.

29 28
33. (currently amended) The ~~apparatus~~ network node of claim 32, wherein ~~said~~ the networking/transport layer further comprises application specific logic that performs ~~said~~ the identifying and ~~said~~ the entering.

30 29
34. (currently amended) The ~~apparatus~~ network node of claim 33, wherein ~~said~~ the application specific logic further comprises a packet processing pipeline that performs ~~said~~ the identifying and ~~said~~ the entering.

31 28
35. (currently amended) The ~~apparatus~~ network node of claim 32, wherein ~~said~~ the networking/transport layer further comprises a processor that performs ~~said~~ the identifying and ~~said~~ the entering via execution of a software program.

37
36. (currently amended) A method for executing a scheduling cycle, comprising:

distributing to each of one or more highest speed grade ~~port~~ports, while counting, permission to release ~~an~~ one of equal amounts ~~amount~~ of data; and

distributing to each of one or more lower speed grade ports, while continuing ~~said~~ the counting, permission to release one of ~~said~~ the equal amounts of data[[,]] until ~~said~~ the counting has counted across a counting modulo, wherein each of ~~said~~ the lower speed grade ~~port(s) consume~~ ports consumes less bandwidth than each of ~~said~~ the one or more highest speed grade ~~port(s), said~~ ports, the counting modulo establishing a temporal width of ~~said~~ the scheduling cycle that results in one of ~~said~~ the equal amounts of data per scheduling cycle being the amount of bandwidth allocated to each of the one ~~of said~~ or more highest speed grade ~~port(s)~~ports.

33 32
37. (currently amended) The method of claim 36, further comprising recognizing ~~said~~ a highest speed grade as an active speed grade prior to ~~said~~ distributing to each of the one or more highest speed grade ~~port~~ ports permission to release ~~said amount~~ the one of equal amounts of data.

34 33
38. (currently amended) The method of claim 37, further comprising, in response to ~~said~~ recognizing ~~said~~ the highest speed grade as ~~said~~ the active speed grade, reading from a memory each data entry within a circular link list, each of ~~said~~ the one or more highest speed grade ports represented by one of ~~said~~ the data entries within ~~said~~ the circular link list, wherein each one of ~~said~~ the data entries has a value used to generate a ~~said~~ permission to ~~the~~ a particular highest speed grade port that ~~it~~ the data entry represents.

35 34
39. (currently amended) The method of claim 38, wherein one of ~~said~~ the data entries has a second value that indicates ~~it~~ that the data entry is the last data entry in

~~said~~ the circular link list, ~~said~~ wherein reading of ~~said~~ the last data entry causing a next lower speed grade to be recognized as the active speed grade.

36 35
40. (currently amended) The method of claim 39, wherein ~~a) said~~ the counting modulo is ~~$x_1$ = min integer[B/X]; where,~~ a minimum integer derived from B divided by X, wherein B is ~~the~~ a switching ~~or routing~~ capacity of a networking system that executes ~~said~~ the scheduling cycle and X is ~~said~~ the amount of bandwidth allocated to each of the one or more ~~one of said~~ highest speed grade ~~port(s); and~~ ports; ~~b) said~~wherein counting across ~~said~~ the counting modulo causes the ~~causing said~~ highest speed grade to be recognized as ~~said~~ the active speed grade for ~~the~~ a beginning of a next scheduling cycle.

37 32
41. (currently amended) The method of claim 36, further comprising recognizing a particular lower speed grade as an active speed grade prior to ~~said~~ the distributing to each of one or more lower speed grade ports permission to release ~~said amount~~ one of the equal amounts of data.

38 37
42. (currently amended) The method of claim 41, further comprising, in response to ~~said~~ recognizing a particular lower speed grade as ~~said~~ the active speed grade, reading from a memory each data entry within a circular link list, wherein each of ~~said~~ the lower speed grade ports that is allocated bandwidth at said particular lower speed grade is represented by one of ~~said~~ the data entries within ~~said~~ the circular link list, wherein each one of ~~said~~ the data entries has a value used to generate a ~~said~~ permission to the specific lower speed grade port that ~~it~~ the data entry represents.

39 38
43. (currently amended) The method of claim 42, wherein one of ~~said~~ the data entries has a second value that indicates ~~it~~ the data entry is ~~the~~ a last data entry in ~~said~~ the circular link list, ~~said~~ wherein reading of ~~said~~ the last data entry causing a next lower speed grade to be recognized as the active speed grade.

40 39
44. (currently amended) The method of claim 43, further comprising keeping track of a different counting modulo for each lower speed grade, wherein ~~said counting modulo is a highest speed grade counting modulo and~~ a lower speed grade counting modulo for ~~said~~ a particular lower speed grade bandwidth ~~allotment(s) is:~~ allocation is ~~$x_n=kx_{n-1}$, where,~~ k times $X_{n-1}$, wherein k is ~~the~~ a number of ~~said~~ particular lower speed grade bandwidth ~~allotment(s)~~ allocations that can be provided by a next highest speed grade, and ~~where~~ wherein $x_{n-1}$ is ~~the~~ a counting modulo for ~~said~~ a next highest speed grade.

41
45. (new) A method for scheduling in a network node, comprising:

(a) setting an active speed grade to a highest speed grade;

(b) servicing as much as possible of a servicing circle of the active speed grade until a count for the highest speed grade has timed out;

(c) if the servicing circle of the active speed grade has been fully serviced and the count for the highest speed grade has not timed out, then setting the active speed grade to a lower speed grade that is a highest speed grade having a servicing circle that has not been fully serviced and going to operation (b) and repeating;

(d) if the count for the highest speed grade has timed out, then setting the active speed grade to the highest speed grade that has not timed out and going to operation (b) and repeating.

42 41
46. (new) The method of claim 45, wherein the servicing circle comprises a plurality of ports of the network node.

43 41
47. (new) The method of claim 45, wherein the servicing circle is represented as a linked list in a memory of the network node.

44 41
48. (new) The method of claim 45, wherein servicing as much as possible of a servicing circle of the active speed grade until a count for the highest speed grade has timed out comprises releasing packets one-by-one identified by a linked list of the servicing circle until the count for the highest speed grade has timed out.